Short Papers

On-Wafer Verification of a Large-Signal MESFET Model

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Abstract—**A relatively simple and new RF measurement procedure is described that is useful for on-wafer, large-signal tests. Predictions using the GaAs FET model agree well with measurements of typical RF gain, gain compression at the fundamental frequency, and the power output at the second and third harmonics.**

I. Introduction

It is desirable to use on-wafer tests to verify the large-signal behavior of GaAs wafers. The procedure described here can be accomplished during RF probing of the PCM (process control monitor). These measurements have been performed using the microwave probe station from Cascade Microtech, Inc., which is used for on-wafer scattering parameter measurements. The tests can be made after front-side processing or after back-side processing and dicing of the wafer.

This work is similar to that of Sango *et al.* [1] in that a FET model is present and verified at RF frequencies. It is significantly different in that the FET model is for a FET process type (designated M05A-2) and was not generated from the actual FET's used for model verification. In addition, the measurement procedure used here is more accurate and has not been reported elsewhere.

This measurement procedure may also be used as a screening method to verify large-signal performance of a wafer before back-side processing.

II. Measurement Procedure

The Cascade microwave probes are used to provide 50 Ω impedance input and output transmission lines for the test FET. Using the equipment configuration shown in Fig. 1, the RF input power is increased in 1 dB steps until the FET has heavy gain compression. At the same time, the output power at fundamental, second harmonic, and third harmonic is measured. It is important to have accurate calibration at each frequency and to include the low-pass filters to avoid ambiguous harmonic effects. The RF loading at fundamental and harmonic frequencies up to 26 GHz is 50 Ω.

The FET devices were biased at 50 percent of I_{dss} and operated at $V_{ds} = 5$ V and 9 V. These data for the power output at fundamental, second- and third-harmonic frequencies from M05A-2 devices were quite similar. Fig. 2 shows the third-harmonic output power for three different FET's.

One advantage of testing the FET in a 50 Ω system is that the power calibration is relatively simple. If matching transformers are used, it is difficult to evaluate accurately the losses of the transformers. One disadvantage of the 50 Ω tests is that the FET is severely mismatched, particularly at the gate or the input port. However, we find that any uncertainty associated with the reflection coefficient at the input does not cause serious error for FET's of 200 μm to 600 μm periphery. The data for the 600 μm FET's are better behaved and are considered to be more accurate.

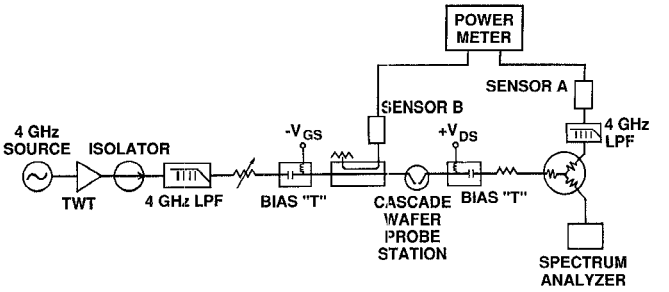

Fig. 1 RF test equipment for saturation test.

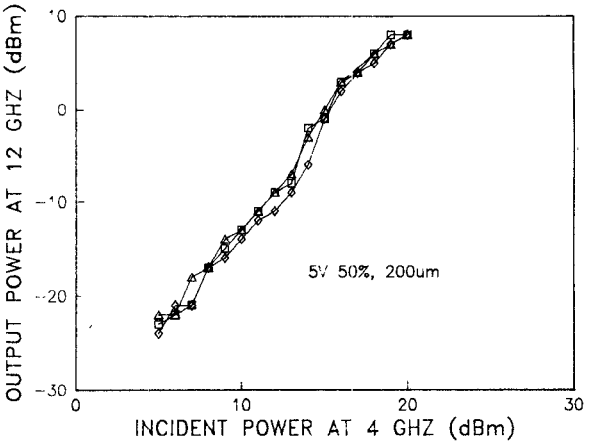

Fig. 2. Third-harmonic RF output power as a function of incident RF power for three FET's under test.

III. FET Model and Simulations

The FET model and parameters used are for the M05A-2 process. This FET process has a nominal gate length of 0.5 μm and an I_{dss} value of 300 mA/mm, and the model used is based upon the work of Curtice and Ettenberg [2]. The model parameters are derived from dc tests, RF scattering parameter tests, and pulsed avalanche breakdown measurements on a large number of chips from many different wafers. *S*-parameter and current–voltage characterization tests are made on the PCM FET's after front-side processing is completed and before final thinning of the wafer. Several wafers in each lot and several lots must be tested to ensure that reliable average parameter values have been found for the FET model. The temperature coefficients for the parameter values are also evaluated during these tests.

The avalanche breakdown behavior of the FET process was also characterized. We found that it was particularly important to

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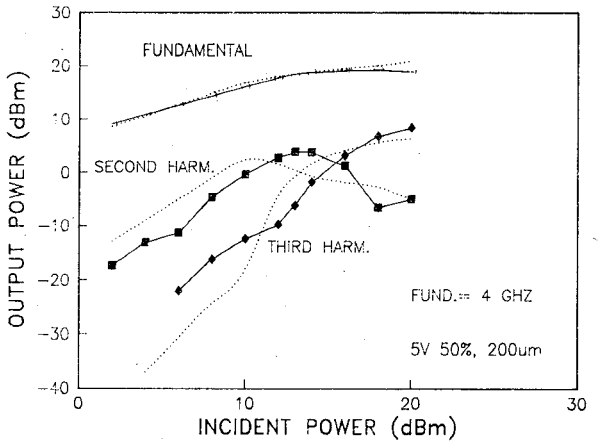

Fig. 3. Output RF powers as a function of incident RF power for typical 200 μm periphery FET at $V_{ds} = 5.0$ V. Solid lines are data; dotted lines are calculated from the large-signal model.

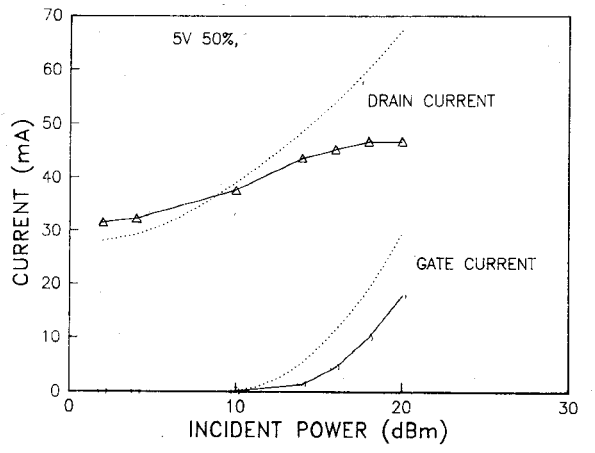

Fig. 4. Drain current and gate current for the same conditions as Fig. 3.

use avalanche coefficients for the correct (elevated) temperature of the channel. In the actual devices tested on-wafer, the RF output power was limited by forward gate conduction, not by the avalanche process.

It is of particular significance that the large-signal RF tests described here are made on FET devices not used in the data base for the process model. In other words, we are not characterizing a FET and then performing large-signal tests on it. We have characterized a FET process and then have tested FET's made by that process.

Simulation of the operation of the device is made using harmonic balance software similar to that available commercially. The FET model behaves well in harmonic balance software, even when bias dependence of the element values is used. This will be discussed further in a later section.

IV. Comparison of the Data with the Simulations

Fig. 3 shows comparison of the data from a typical device (points) and the simulation results (dotted lines) using the M05A-2 foundry model for 5 V drain–source operation. The output power at the fundamental agrees very well, whereas the agreement at the second and third harmonic is reasonable but not as good. Fig. 4 compares the data and the model for the drain and gate currents for the same device. The gate current is due to forward gate conduction because of the large RF input voltage. Some differences between the model and the real device can be traced to the real device having a pinch-off voltage about 0.5 V larger. This is the reason for the difference in the increase in the drain current in Fig. 4. Measurements at 9 V operation showed about the same agreement.

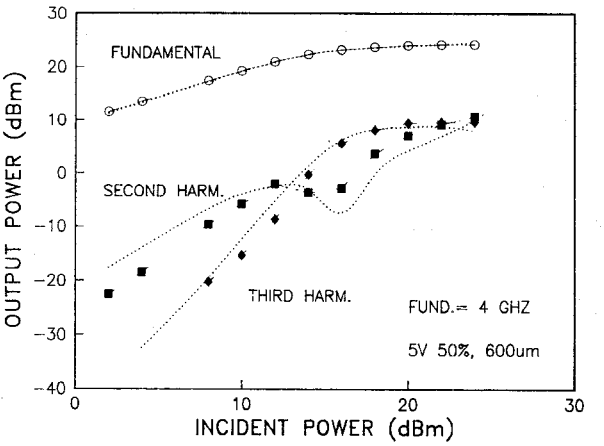

Fig. 5. Output RF powers as a function of incident RF power for one 600 μm periphery FET at $V_{ds} = 5.0$ V. Solid lines are data; dotted lines are calculated.

Fig. 5 shows a comparison of RF power for the data on a larger FET, of 600 μm periphery. Again, the agreement of the fundamental output power is excellent. The agreement for the second- and third-harmonic output power is better than for the smaller device. One reason is the improved accuracy of measurement, as stated earlier. It is satisfying to observe that the model's prediction of third-harmonic power behavior with drive power is significantly different for the two device sizes, in agreement with the measurements. For example, notice that for the 200 μm device, the third-harmonic power is much less than the second-harmonic power at 20 dBm input, whereas for the 600 μm device, the third-harmonic power is equal to the second-harmonic power at 20 dBm input power. Both the model and the data exhibit this same behavior.

V. Bias-Dependent Model Elements

As discussed in the earlier study [2], the inclusion of the bias dependency of C_{gs} and C_{dg} produces only small effects upon the RF saturation characteristics at the fundamental frequency. However, we find significant effects at the second- and third-harmonic frequencies. Fig. 6 shows the same data as Fig. 5 and the "simple model" which does not include the bias dependencies of C_{gs} and C_{dg}. Fig. 6 shows that the simple model overestimates the second-harmonic output at low input power and underestimates the third-harmonic output at low input power. At high input power, the second-harmonic output is underestimated and the third-harmonic output is in reasonable agreement. No significant change occurred in the fundamental-frequency output in Fig. 6. The simulation results for the simple FET model presented in Fig. 6 are very close to the computational results obtained using LIBRA [3] with the LEVEL 2 FET model.

VI. Conclusion

A relatively simple and new RF measurement procedure that can be made on wafer has been shown to verify the MSC foundry model for test FET's. The nonlinear FET model agrees well with the measured devices with respect to the gain, gain compression at fundamental frequency, and power output at second and third harmonics. It is particularly significant that these test chips were not used in earlier measurements made to develop the model.

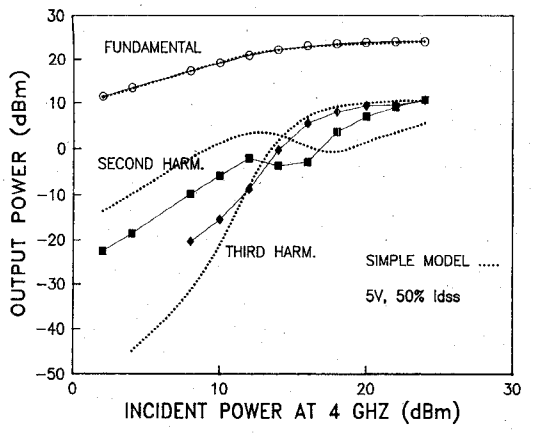

Fig. 6. Output RF powers as a function of incident RF power for the same device as in Fig. 5. Solid lines are data and dashed lines are calculated from FET model not including bias dependencies of C_{gs} and C_{dg}.

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[2] W. R. Curtice and M. Ettenberg, "A nonlinear GaAs FET model for use in the design of output circuits for power amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, pp. 1383–1394, Dec. 1985.

[3] *LIBRA*, EEsof, Inc., Westlake Village, CA.

A Low-Noise Microwave Oscillator Employing a Self-Aligned AlGaAs/GaAs HBT

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***Abstract*—This paper studies the application of heterojunction bipolar transistors (HBT's) to low-noise microwave circuits. Design considerations and the low-noise performance of a *Ku*-band free-running oscillator using a self-aligned AlGaAs/GaAs HBT are described. The device has a novel structure in which by utilizing SiO_2 sidewalls the base surface area, which is the main cause of low-frequency noise, is drastically reduced. For a collector current of 1 mA, the fabricated device has base current noise power densities of 4×10^{-20} A²/Hz, 6×10^{-21} A²/Hz, and 2.5×10^{-21} A²/Hz at baseband frequencies of 1 kHz, 10 kHz, and 100 kHz, respectively. The prototype oscillator operating at 15.5 GHz has a measured output power of 6 dBm and SSB FM noise power densities of −34 dBc/Hz at 1 kHz, −65 dBc/Hz at 10 kHz, and −96 dBc/Hz at 100 kHz off-carrier, respectively, without employing any high-Q elements such as a dielectric resonator. The results of this study demonstrate the suitability of HBT's for low-phase-noise microwave and millimeter-wave oscillator applications.**

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I. Introduction

With rapid advances in microwave communication technology, there is increasing demand for low-phase-noise oscillators operating at microwave frequencies. Oscillators fabricated with GaAs FET's suffer from a high level of phase noise [1]. This noise results from the baseband noisy characteristics of the device due to large amounts of free-surface, depletion-layer, and channel–substrate interface trap centers.

Oscillators fabricated with Si bipolar transistors, which are only available up to about 20 GHz, show excellent noise behavior [2], [3] since the device has a vertical structure and features a very small number of recombination trap centers. On the other hand, continuing progress in compound semiconductor crystal growth technology has led to the development of heterojunction bipolar transistors (HBT's) which, when compared with GaAs FET's and Si bipolar transistors, promise superior applicability to microwave oscillator circuits with appreciably low noise performance.

The present paper is concerned with the application of AlGaAs/GaAs HBT's to low-phase-noise *Ku*-band oscillators.

II. Phase Noise Generation in Oscillators

The phase noise spectral density $S_\phi(\omega)$ for a microwave oscillator operating at a frequency ω_0 with an RF current amplitude A_0 in terms of the low-frequency noise spectral density $S_{LF}(\omega_b)$, the device impedance $-Z_d(A)$, and the circuit impedance $Z_c(\omega)$ can be given by [4]

$$S_\phi(\omega_b) = \left[\frac{w_b\left|\frac{dZ_c(\omega)}{d\omega}\right|_{\omega_0}^2+\left(A_0^2/\omega_b\right)\left|\frac{\partial Z_d(A)}{\partial A}\right|_{A_0}^2}{A_0^2\omega_b^2\left|\frac{dZ_c(\omega)}{d\omega}\right|_{\omega_0}^4+A_0^2\left|\frac{dZ_c(\omega)}{d\omega}\right|_{\omega_0}^2\left|\frac{\partial Z_d(A)}{\partial A}\right|_{A_0}^2\sin^2\theta}\right]\cdot S_{LF}(\omega_b) \quad (1)$$

with

$$S_{LF}(\omega_b) \equiv \langle i_{LF}^2\rangle/\text{Hz} = \frac{\lambda(T)A_0^\alpha}{\omega_b^\beta} \quad (2)$$

where $\langle i_{LF}^2\rangle$ represents the device low-frequency noise current power spectrum, $\lambda(T)$ is a temperature-dependent proportionality factor, ω_b is the baseband frequency, θ is the device line $Z_d(A)$ and impedance locus $Z_c(\omega)$ intersecting angle at (ω_0, A_0), $\alpha \simeq 2$, and $\beta \simeq$ [5], [6]. With respect to (1) and (2), the oscillator phase noise is an up-conversion of the active device low-frequency noise into the carrier frequency through an interaction of the active device with the passive circuit.

To achieve a low-phase-noise oscillator it is, therefore, of prime importance to employ devices demonstrating low $1/f$ noise. The $1/f$ noise behavior for a microwave transistor is strongly influenced by the device structure and by the factor λ in (2). The principal mechanisms for the generation of low-frequency noise in lateral structure devices such as GaAs FET's are (i) the interaction of carriers with traps in the oxide near the source–gate and gate–drain free surface region, which results in the surface mobility fluctuation; (ii) generation–recombination (G–R) traps in the gate/channel depletion region; and (iii) traps at the channel–substrate interface [7]. In the case of vertical-structure